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Colorado State University's Information Science and Technology Center (ISTeC)

presents two lectures by

Dr. Jean-Luc Gaudiot

Professor and Chair, Electrical Engineering and Computer Science
University of California - Irvine

ISTeC Distinguished Lecture

in conjunction with the Computer Science Department Seminar Series

"The Walls of Computer Design"

Monday, October 9, 2006
Reception: 10:00 a.m. to 11:00 a.m.
Engineering Internet Café, Engr room A104
Lecture: 11:00 a.m. to 12:00 noon
Shepardson room 118

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Joint Electrical and Computer Engineering Department and Computer Science Department Lecture

sponsored by ISTeC

"Design and Effectiveness of Small Decoupled Dispatch Queues"

Tuesday, October 10, 2006
Lecture: 9:30 a.m. to 10:30 a.m.
Wagar room 132

ABSTRACTS

"The Walls of Computer Design"

Most of the work of the computer architect today has to do with bridging the well-known gigantic gap between processor speed and memory access time. However, other significant challenges are looming on the horizon. For one thing, higher device density and smaller design rules are increasing the sensitivity of circuits to outside radiation events. Also, power issues are creating significant challenges, not only in terms of power consumption for embedded devices, but also in terms of cooling and power dissipation. Hence, while Moore's law will continue to hold for the foreseeable future (every two years see a 1.5-fold increase in the number of devices available on a chip), processor speeds are not expected to follow suit, thereby requiring new architectural concepts. In this lecture, we will describe the issues surrounding modern computer architecture and design. We will discuss the advent of newer architectures such as multi-core chips and examine the associated synchronization problems, implementation issues, and performance evaluation considerations. We also will study the implications of power considerations and demonstrate scheduling approaches to control consumption and heat dissipation. Redundant thread execution will be demonstrated as a simple synchronization method that offers low cost protection against the Single Event Upsets (SEUs) plaguing modern systems with increasing frequency.

"Design and Effectiveness of Small Decoupled Dispatch Queues"

Continuing demands for high degrees of Instruction Level Parallelism (ILP) require large dispatch queues in modern superscalar microprocessors. However, such large queues are inevitably accompanied by high circuit complexity that correspondingly limits the pipeline clock rates. This is due to the fact that most of today's designs are based upon a centralized dispatch queue that depends on globally broadcasting operations to wakeup and select the ready instructions. As an alternative to this conventional design, we propose the design of hierarchically distributed dispatch queues, based on the access/execute decoupled architecture model. Simulation results based on 14 data intensive benchmarks show that our DDQ (Decoupled Dispatch Queues) design achieves performance comparable to a superscalar machine with a large dispatch queue. We also show that our DDQ can be designed with small-sized, distributed dispatch queues that consequently can be implemented with low hardware complexity and high clock rates.

SPEAKER BIOGRAPHY

Dr. Jean-Luc Gaudiot (http://pascal.eng.uci.edu/people/gaudiot.html) received the Diplôme d'Ingénieur from the École Supérieure d'Ingénieurs en Electronique et Electrotechnique, Paris, France in 1976 and the M.S. and Ph.D. degrees in Computer Science from the University of California, Los Angeles in 1977 and 1982, respectively. He is currently a Professor in the Electrical Engineering and Computer Science Department at the University of California, Irvine. Prior to joining UCI in January 2002, he was a Professor of Electrical Engineering at the University of Southern California since 1982, where he served as Director of the Computer Engineering Division for three years. He has also designed distributed microprocessor systems at Teledyne Controls, Santa Monica, California (1979-1980) and performed research in innovative architectures at the TRW Technology Research Center, El Segundo, California (1980-1982). He frequently acts as consultant to companies that design high-performance computer architectures, and has served as an expert witness in patent infringement and product liability cases. His research interests include multithreaded architectures, fault-tolerant multiprocessors, and implementation of reconfigurable architectures. He has published over 150 journal and conference papers. His research has been sponsored by NSF, DoE, and DARPA, as well as a number of industrial organizations. In January 2006, he became the first Editor-in-Chief of the IEEE Computer Architecture Letters, a new publication of the IEEE Computer Society, which he helped found to the end of facilitating short, fast turnaround of fundamental ideas in the Computer Architecture domain. From 1999 to 2002, he was the Editor-in-Chief of the IEEE Transactions on Computers. In June 2001, he was elected chair of the IEEE Technical Committee on Computer Architecture, and re-elected in June 2003 for a second two-year term.

To meet with the speaker, contact MaryAnn Stroub at (970) 491- 2708 or mstroub@engr.colostate.edu

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