ISTeC



Colorado State University

The Information Science & Technology Center

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Colorado State University's Information Science and Technology Center (ISTeC)

presents <u>two</u> lectures by

Dr. Mike Flynn

Senior Adviser, Maxeler Corp. and
Professor Emeritus, Stanford University

ISTeC Distinguished Lecture

in conjunction with the
Electrical and Computer Engineering Department and
Computer Science Department Seminar Series

"Super SOC: Putting the Whole System on the Chip"

Monday, November 12, 2007
Reception: 10:30 a.m.
Lecture: 11:00 – 12:00 noon
Lory Student Center Room 228

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Joint Electrical and Computer Engineering Department and Computer Science Department Special Seminar
sponsored by ISTeC

"The Future is Parallel But it May Not be Easy"

Tuesday, November 13, 2007
Lecture: 9:30 – 10:30 a.m.
Natural Resources Room 109

ABSTRACTS

“Super SOC: Putting the Whole System on the Chip”
With dramatic advances in transistor density, it's time to look ahead to the completely autonomous system on a single die (ASOC). This represents a convergence of RFID type technology with SOC silicon technology coupled with silicon transducers, sensor controllers and battery, all on the same die. The major architectural implication is design for extremely low power (1 microwatt or less) and strict energy budget. This requires a rethinking of clocking, memory organization, and processor organization. The use of deposited thin film batteries, extremely efficient RF, digital sensors and MEMS (micro-electro-mechanical systems) complete the ASOC plan.

“The Future is Parallel But it May Not be Easy”
Processor performance scaling by improving clock frequency has now hit power limits. The new emphasis on multi core architectures comes about from the failure of frequency scaling not because of breakthroughs in parallel programming or architecture. Progress in automatic compilation of serial programs into multi tasked ones has been slow. A look at parallel projects of the past illustrates problems in performance and programmability. Solving these problems requires both an understanding of underlying issues such as parallelizing control structures and dealing with the memory bottleneck. For many applications performance comes at the price of programmability and reliability comes at the price of performance.

SPEAKER BIOGRAPHY

Michael Flynn (http://arith.stanford.edu/~flynn/) began his engineering career at IBM as a designer of mainframe computers. He became Professor of Electrical Engineering at Stanford in 1975 where he set up the Stanford Architecture and Arithmetic group. He retired from Stanford in 1999. Some of his best-known work includes the development of the now familiar stream outline of computer organization (SIMD, etc.). For more than 30 years this has served as the fundamental formal taxonomy of parallel computers. In 1970 he co-authored the first detailed discussion of techniques for the simultaneous execution of multiple instructions, now called super scalar design. He is a Fellow of the ACM and a Fellow of the IEEE.
He is now Emeritus Professor at Stanford and Senior Advisor (and Board Chair) to Maxeler, a London based computation accelerator company.

To arrange a meeting with the speaker, please contact MaryAnn Stroub at (970) 491-2708
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ISTeC (Information Science and Technology Center) is a university-wide organization for promoting, facilitating, and enhancing CSU’s research, education, and outreach activities pertaining to the design and innovative application of computer, communication, and information systems. For more information please see ISTeC.ColoState.edu.