ISTeC
The Information Science and Technology Center

Colorado State University

Distinguished Lectures

Spring 2016

Colorado State University's Information Science and Technology Center (ISTeC) ***presents two lectures by***

Dr. Jean-Luc Gaudiot

2017 IEEE Computer Society President
Professor
Department of Electrical Engineering and Computer Science
University of California - Irvine

ISTeC Distinguished Lecture

In conjunction with the Department of Electrical and Computer Engineering, and Department of Computer Science Seminar Series

"Technology Considerations in Computer Architecture"

Monday, May 2, 2016
Reception with refreshments: 10:30 a.m.
Lecture: 11:00 a.m.-12:00 noon
Morgan Library Event Hall

Department of Electrical and Computer Engineering, and Department of Computer Science Special Seminar *Sponsored by ISTeC*

"SPARTA: A Dataflow-Inspired System Design"

Monday, May 2, 2016
Lecture: 4:00-5:00 p.m.
Engineering Building room B 101

Abstracts

Technology Considerations in Computer Architecture

Good engineering practice uses the characteristics of existing technologies to optimize implementation. Often, this will mean that design techniques optimal in a previous generation prove impractical or even unusable when a new technology becomes dominant. This rule is all too often forgotten, which we will demonstrate in two problems of computer design: Field-Programmable Gate Arrays (FPGAs) and hardware prefetchers (providing the ability to fetch data early in anticipation of the need). FPGAs are extremely useful in mobile embedded systems where computing power and energy considerations are major concerns. Partial reconfiguration is often used to reduce power consumption when parts of the array are inactive, albeit at the cost of high energy overhead due to the large cost of transferring configuration information. Our study reveals that partial reconfiguration accelerates execution and reduces overall energy consumption by half. Second, we will demonstrate how increased transistor integration allows hardware prefetching to improve both energy-efficiency and performance.

SPARTA: A Dataflow-Inspired System Design

Computer systems have undergone a fundamental transformation recently, from single-core processors to devices with increasingly higher core counts within a single chip. The semi-conductor industry now faces the infamous power and utilization walls. To meet these challenges, heterogeneity in design, both at the architecture and technology levels, will be the prevailing approach for energy efficient computing as specialized cores, accelerators, etc., can eliminate the energy overheads of general-purpose homogeneous cores. However, with future technological challenges pointing in the direction of on-chip heterogeneity, and because of the traditional difficulty of parallel programming, it becomes imperative to produce new system software stacks that can take advantage of the heterogeneous hardware. As a case in point, the core count per chip continues to increase dramatically while the available on-chip memory per core is only getting marginally bigger. Thus, data locality, already a must-have in high-performance computing, will become even more critical as memory technology progresses. In turn, this makes it crucial that new execution models be developed to better exploit the trends of future heterogeneous computing in many-core chips. To solve these issues, we propose a cross-cutting cross-layer approach to address the challenges posed by future heterogeneous many-core chips.

Speaker Biography

Jean-Luc Gaudiot received the Diplôme d'Ingénieur from ESIEE, Paris, France, in 1976, and the M.S. and Ph.D. degrees in Computer Science from UCLA in 1977 and 1982, respectively. He is currently a Professor in the Electrical Engineering and Computer Science Department at University of California, Irvine. Prior to joining UCI in 2002, he was a Professor of Electrical Engineering at the University of Southern California since 1982. His research interests include multithreaded architectures, fault-tolerant multiprocessors, and implementation of reconfigurable architectures. He has published over 250 journal and conference papers. His research has been sponsored by NSF, DoE, and DARPA, as well as industry. He has served the community in various positions and was just elected to the presidency of the IEEE Computer Society for 2017. He is a Fellow of the IEEE and a Fellow of the AAAS.

To arrange a meeting with the speaker, please contact Prof. H.J. Siegel, HJ@ColoState.edu.

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