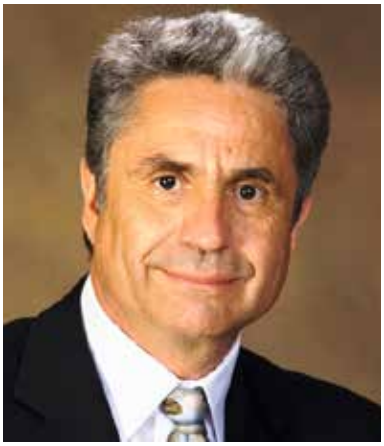

Colorado State University's
Information Science and Technology Center (ISTeC)
presents two lectures by

Ahmed Louri

Professor of Electrical and Computer Engineering,
Director of the High Performance Computing Architectures and Technologies Laboratory,
University of Arizona

ISTeC Distinguished Lecture

In conjunction with the
Electrical and Computer Engineering Department and
Computer Science Department Seminar Series

"Power-Efficient and Reliable Multicore Architectures"

Monday, April 6, 2015
Reception with refreshments: 10:30 am
Lecture: 11:00 am – 12:00 noon
Location: Morgan Event Hall

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Electrical and Computer Engineering Department and Computer Science Department
Special Seminar Sponsored by ISTeC

"Roundtable Discussion: Interacting with Federal Funding ?ec lagcq"

Monday, April 6, 2015
Lecture: 3:00 pm – 4:00 pm
Location: LSC 372-374

ISTeC (Information Science and Technology Center) is a university-wide organization for promoting, facilitating, and enhancing CSU's research, education, and outreach activities pertaining to the design and innovative application of computer, communication, and information systems. For more information please see ISTeC.ColoState.edu.

Abstracts

Power-Efficient and Reliable Multicore Architectures

Today's microprocessor designers have been increasing the number of cores per die as a power-efficient approach to performance improvement, leading to the Chip Multiprocessors (CMPs) or the multicore era. Both industrial and academic roadmaps project that tera-operations per second CMPs will be needed within a decade to satisfy the nation's needs for high-performance computing. The proliferation of multiple cores on the same die heralded the advent of communication-centric designs, rather than computation-centric systems. The on-chip interconnect fabric connecting various modules, namely the processing cores, cache banks, memory units, and I/O devices, has become extremely important. Multicore designs have adopted a flexible and scalable packet-switched architecture called Network-on-Chip (NoC) architecture. Prof. Louri will present several research challenges facing multicore architectures and NoC design (e.g., power dissipation and reliability), and some of his group's ongoing efforts to address them. The talk will conclude with future research directions.

Roundtable Discussion: Interacting with Federal Funding Agencies

Prof. Louri will lead a round table discussion about best practices for interacting with federal funding agencies. He will discuss his experiences as a research grant proposal writer and as a funding agency rotator who helps evaluate proposals, including his recent experience in federal funding management and lessons learned from this. CSU faculty are invited to join in to the conversation with their experiences of what has worked when they have tried to get funding, and what has not. Prof. Louri has led similar round table discussions at other institutions, and they have been very successful.

Speaker Biography

Ahmed Louri received the M.S. and Ph.D. degrees in Computer Engineering from the University of Southern California, Los Angeles, in 1984 and 1988, respectively. He joined the University of Arizona in 1988, where he is currently a Professor of Electrical and Computer Engineering and the Director of the High Performance Computing Architectures and Technologies Laboratory. From 2010 to 2013, he served as a Program Director in the Directorate for Computer and Information Science and Engineering (CISE) of the National Science Foundation with an annual research portfolio of $800 million. He managed the core computer architecture program and was on the management team of several cross-cutting programs including Cyber-Physical Systems (CPS), Expeditions in Computing (EIC), Computing Research Infrastructure (CRI), Trustworthy Computing (SaTC), and Failure-Resistant Systems (FRS). His primary research interests include computer architecture, parallel and distributed computing, interconnection networks, optical interconnects for parallel computing systems, reconfigurable computing systems, scalable and power-efficient architectures, fault-tolerant multiprocessors, Network-on-Chip for multi-core architectures, cognitive architectures, emerging interconnect technologies for multicores, embedded and SoC systems. He has published more than 125 journal articles and conference papers in these areas, and holds several US patents. He is a Fellow of IEEE.

To arrange a meeting with the speaker, please contact Prof. H.J. Siegel, HJ@ColoState.edu.