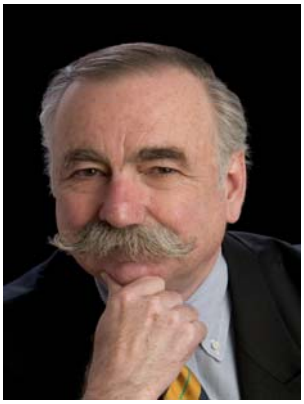
Colorado State University's
Information Science and Technology Center (ISTeC)
presents <u>two</u> lectures by



Dr. T. W. (Tom) Williams

Synopsys Fellow, Synopsys, Inc.

Electrical and Computer Engineering Distinguished Lecture
and *ISTeC Distinguished Lecture*

"Electronic Design Automation (EDA) to the Rescue of the Silicon Roadmap"

Monday, March 24, 2008
Reception: 8:30 – 9:00 a.m.
Lecture: 9:00 – 10:00 a.m.
Location: Lory Student Center Room 222

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Joint Electrical and Computer Engineering Department and Computer Science Department Special Seminar

sponsored by ISTeC

"Quality Now Requires Small Delay Fault Model"

Tuesday, March 25, 2008
Lecture: 12:30 – 1:30 p.m.
Location: Engineering Room B103

ABSTRACT

“Electronic Design Automation (EDA) to the Rescue of the Silicon Roadmap”

Since the invention of the transistor nearly six decades ago, new technology nodes have been added approximately every two years, yielding smaller transistors that run about 40% faster with each geometry scaling. Now, in the realm of 65- and 45-nanometer design and manufacturing, the industry is confronted by multiple complex challenges: silicon technology keeps shrinking, but doesn't advance in speed at the same rate. We are driving to the edge of the silicon roadmap, but there is no viable alternative to CMOS within our reach. Not coincidentally, several companies are announcing their intention to stop internal R&D at the 45 nanometer node and use foundry-supplied processes at 32 nanometers and below. The electronics industry ecosystem is at a fork in the road: those few who can afford it will keep rushing to 45 nanometers and beyond; the rest will hold at 130 or perhaps 90 nanometers. In both cases it is EDA that will come to the rescue. Advanced EDA provides a competitive advantage at 90 nanometers and above, and is a matter of plain survival at 65 nanometers and below. EDA innovation is the gear that enables design for low power, design for manufacturing and yield (which encompasses design for test), and design for variability.

“Quality Now Requires Small Delay Fault Model”

The concept of small delay faults has been discussed for more than 20 years. Methods for determining the relative merits of delay test sets have also been known for 20 years. Until recently this area of testing has been considered unnecessary. Today many groups want to use small delay fault testing to achieve high quality levels. This lecture will address the derivation of quality metrics and how they are used today. Testing for small delay defects requires ATPG-FS tools to understand timing information of the design such that transition delay faults can be detected along longer paths. Timing information is analyzed for use in test automation tools to test for small delay defects. Fundamentals of static timing analysis are analyzed with regard to the test procedure. This lecture shows that Signal Integrity information can be ignored by test automation tools when timing information is used to guide ATPG tools towards longer paths. This work also shows that a lack of understanding of clock trees in the long path ATPG algorithm leads to incorrect results.

SPEAKER BIOGRAPHY

Dr. Thomas W. Williams is a Synopsys Fellow at Synopsys in Boulder, Colorado, U.S.A. Formerly, he was with the IBM Microelectronics Division and manager of the VLSI Design for Testability group. He received a B.S.E.E. from Clarkson University, an M.A. in pure mathematics from the State University of New York at Binghamton, and a Ph.D. in electrical engineering from Colorado State University. He has received numerous best paper awards from the IEEE and ACM and was twice a Distinguished Visitor lecturer for the IEEE Computer Society. Dr. Williams has previously served on the Computer Society Board of Governors and the IEEE Board of Directors, and was the Society's 2000 Treasurer. He is a member of the Eta Kappa Nu, Tau Beta Pi, IEEE, ACM, Sigma Xi, and Phi Kappa Phi. He is an Adjunct Professor at the University of Calgary, Calgary, Alberta, Canada. Dr. Williams was named an IEEE Fellow in 1988 and received the Computer Society W. Wallace McDowell Award for outstanding contributions to the computer art in 1989. He was named a member of the Chinese Academy of Science. In 2007, Dr. Williams received the European Design and Automation Association Lifetime Achievement Award for **“**outstanding contributions to the state of the art in electronic design, automation, and testing of electronic systems.**”**

To arrange a meeting with the speaker, please contact MaryAnn Stroub at (970) 491-2708 or mstroub@engr.colostate.edu.

ISTeC (Information Science and Technology Center) is a university-wide organization for promoting, facilitating, and enhancing CSU’s research, education, and outreach activities pertaining to the design and innovative application of computer, communication, and information systems. For more information please see ISTeC.ColoState.edu.